SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech I Year II Semester Supplementary Examinations May-2022 ELECTRONIC DEVICES AND CIRCUITS

(Electrical and Electronics Engineering)

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|----------|----------------------|--|--------|-----------|
| T | ime: 3 ho | ours | lax. M | larks: 6 |
| (Ar | swer all | Five Units $5 \times 12 = 60$ Marks) | | |
| | | UNIT-I | | |
| 1 | a Draw | the ideal diode characteristics and give its circuit symbol. | L1 | 4M |
| | | nine the forward resistance of a PN junction diode when the forward current is at $T = 300$ K. Assume Silicon diode. | L4 | 4M |
| | c Defin | ne Breakdown voltage and give the circuit symbol for Zener Diode. OR | L2 | 4M |
| 2 | | rate the action of PN junction diode under forward bias and reverse bias and h its V-I Characteristics. | L2 | 6M |
| | b What diagra | is a Clamper circuit? Describe positive and negative clampers with neat circuit ams. | L1 | 6M |
| | | UNIT-II | | |
| 3 | | ct the expressions for Average DC current, Average DC Voltage, RMS Value rrent, DC Power Output and AC Power input of a Half Wave Rectifier. | L4 | 6M |
| | | the circuit diagram of a Full wave rectifier and with the help of waveforms ibe its operation. | L1 | 6M |
| OR | | | | |
| 4 | | neat circuit diagram and waveforms, illustrate the construction and working of se rectifier. | L2 | 4M |
| | | ct the construction and working principle of CLC or π section filter along with ation for its ripple factor. | L4 | 8M |
| UNIT-III | | | | |
| 5 | a Interp | oret the operation of NPN transistor with a neat diagram. | L2 | 6M |
| | b With | neat diagram, Interpret the Input and Output characteristics of a BJT in CB guration. | L2 | 6M |
| | | OR | | |
| 6 | | base current in a transistor is $20\mu A$ when the emitter current is 6.4mA, what e values of α and β ? Also calculate the collector current. | L1 | 6M |
| | b Comp | pare the performance of JFET with MOSFET. UNIT-IV | L2 | 6M |
| 7 | a Defin | e Transistor Biasing and explain the need for Biasing. | L1 | 6M |
| | | in Collector to Base bias of a Transistor with neat circuit diagram. | L2 | 6M |
| | | | | |

OR

- 8 a Define Stability Factor S. Derive the stability factor S for collector to base bias of BJT.
 b An NPN Transistor if β = 50 is used in common emitter circuit with VCC=10V and L3 6M
 - **b** An NPN Transistor if $\beta = 50$ is used in common emitter circuit with VCC=10V and RC= 2K Ω . The bias is obtained by connecting 100K Ω resistor from collector to base. Find the Quiescent point and stability Factor.

UNIT-V

- 9 a Examine the expressions for current gain, voltage gain, input impedance and output L4 6M impedance of CB amplifier using simplified hybrid model.
 - **b** A voltage source of internal resistance, $Rs = 900\Omega$ drives a CC amplifier using load resistance $RL=2000\Omega$. The CE h parameters are hfe=60, hie=1200 Ω , hoe = 25 μ A/V and hre = 2 x 10-4. Solve AI, Ri, Av and R0 using approximate analysis.

OR

- **10** a Determine the parameters Ai, Ri, Av and R0 of Common Collector Amplifier using **L5** 6M simplified hybrid model analysis.
 - b Develop the expression for current gain, voltage gain, input impedance and output impedance for Common Emitter Amplifier with Emitter Resistor using simplified hybrid model.

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